

SLOBODNIK et al  
Appl. No. 10/025,816  
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**AMENDMENTS TO THE SPECIFICATION:**

Page 9, amend the paragraph beginning at line 16 as follows:

Figure 4 schematically illustrates a mapping of physical memory address signals to logical memory address signals; and

Page 9, amend the paragraph beginning at line 19 as follows:

Figure 5 illustrates in more detail a particular example of an address signal mapping that may be required;

Figure 6 schematically illustrates an MBIST user interface; and

Figure 7 schematically illustrates an MBIST instruction register.

Page 15, delete the text beginning at line 20 which starts with "Contents" and ends at line 34 ("2.4.3. Pattern/Algorithm selection <9:4>.....").

Please delete pages 16-27 and substitute therefor the attached specification pages 16-32.